PHISON

The Ultimate PCIe Gen3 Solution

Phison PS5015-E15T (Phison E15T) is the ultimate PCIe Gen3 NAND flash controller IC solution providing incomparable performance on the Gen3 interface with unmatched power efficiency and cost effectiveness. The E15T is the final station in the PCIe Gen3 DRAM-less swim lane boasting higher performance and lower power consumption than low-end Gen4 solutions while its DRAM-less design gives it an edge in cost competitions.

Application

PCIe Gen3 Client Platforms

Mainstream Game Consoles

PHISON PS5015-E15T

Product Features

Unmatched Cost-effectiveness

As a refreshed, fully mature DRAM-less PCIe Gen3 solution, the E15T retains top-notch performance reaching above 3400MB/s in sequential operations while enabling compelling cost-savings to create invaluable design-in opportunities in cost-sensitive consumer markets.

Superb Power Efficiency

Phison E12/E12S supports up to 8 flash channels with 32 Chip Enable (CE) counts on both of the mainstream NAND flash interfaces in ONFI and Toggle, allowing capacity scaling from 512 GB up to 8 TB.

Host Memory Buffer (HMB)

Phison E15T supports the Host Memory Buffer (HMB) feature, which creates a path for the an SSD to leverage some portion of the host system memory as the device's own buffering cache, and bypasses the use of costly on-board DRAMs .

End-to-End Data Path Protection

From the entry through PHY to the access of NAND flash memory, data packages go through a series of encryption/decryption using various coding schemes, including but not limited to AES, CRC, and SEDEC, to gain a multi-layered protection over the course of delivery.

CONTROLLER
PS5015-E15T

Features	Specifications
Host Interface	- PCIe 3.0 x4 (Bandwidth: 8GT/s x4) - Backward compatible with existing PCIe generation transfer rates - Compliance with PCI Express Base Specification Revision 3.1 - Compliance with NVMe 1.4 - Host Memory Buffer (HMB) support
Processor	- Single CPU architecture - TSMC 28nm process technology
Flash Controller	- Up to 4 Channels with 16 chip enable (CE) counts - Flash transfer rate up to 1200MT/s - Capacity up to 2TB - Support 3D TLC NAND flash memory - Compliance with Toggle 4.0 and ONFi 4.2 - Flash I/O operating voltage supply 1.2V/1.8V
Data Reliability	- Phison 4th generation LDPC ECC & RAID ECC - End-To-End Data Path Protection
Security	- Pyrite - AES 256 - SHA 512 - RSA 2048
Performance	- Sequential Read up to 3400MB/s - Sequential Write up to 3000MB/s - 4K Random Read up to 500K IOPS - 4K Random Write up to 720K IOPS
Power Management	- L1.2 < 5mW
Temperature Range	- Operating range: 0~70 °C - Storage range: -40~85 °C
Package	- 198-ball HSTFBGA, 7mm x 11mm
Peripheral	- Built-in internal thermal sensor - GPIO pins - Built-in UART function - I2C and SPI for external ROM

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Find more information and resources at: **phisonblog.com** and **phison.com**

Solutions

PS5015-E15T

Capacity[1]	250/256 GB	500/512 GB	1000/1024 GB	2000/2048 GB
Interface	PCIe Gen3.0x4 NVMe 1.4			
Form Factor	M.2 2280-S2			M.2 2280-D2
NAND Flash	3D TLC			
Performance [2,3]				
Sequential Read	3300 MB/s	3400 MB/s	3300 MB/s	3300 MB/s
Sequential Write	1700 MB/s	3000 MB/s	3000 MB/s	3000 MB/s
4K Random Read	400K IOPS	400K IOPS	430K IOPS	400K IOPS
4K Random Write	600K IOPS	700K IOPS	700K IOPS	600K IOPS
Power [4]				
Supply Voltage	M.2 3.3V ± 5%			
Active (Average)	3400 mW	3400 mW	4000 mW	4000 mW
Low Power PS4 (L1.2)	5 mW	5 mW	5 mW	5 mW
Environmental				
Operating Temperature	0°C - 70°C			
Non-Operating Temperature	-40°C - 85°C			
Reliability & Warranty				
TBW[5]	150 TB	300 TB	600 TB	1200 TB
MTBF	1.5 million hours			
UBER	$<10^{-16}$ bits			
Advanced Features				
- End-to-End Data Protection - Pyrite Support - Thermal Monitoring				

(1) 1 GB = 1,000,000,000 bytes
(2) Sequential Performance is based on CrystalDiskMark 6.0, 1GB range, QD=32T1 , and test drive set as secondary
(3) Random Performance is based on IOMeter, 1GB range, 4K data size, QD=32T16, 4K aligned
(4) Power consumption is measured during the sequential read and write operations performed by CrystalDiskMark with the conditions described in (3)
(5) TBW is Total Bytes Written and the results are obtained in compliance with JESD218 Standards

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