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PHISON PS7202  
PCIe 5.0 RETIMER IC  
DATASHEET

V2.3 Mar. 3, 2026

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## REVISION HISTORY

Revision	Description	Draft Date
1.0	● Initial release	Oct 06, 2023
2.2	● Modify Public version	Mar. 20, 2025
3.3	● Minor update	Mar. 3, 2026

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## About Us

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Phison Electronics Corporation was established in November 2000 in Hsinchu, Taiwan. Starting with the world's first single-chip USB flash drive IC, Phison is now a market leader in NAND Flash controllers and high speed interface IC including retimer and redrivers. The company has shipped million NAND controllers and high speed interface IC solutions worldwide. As a ASIC solution provider, Phison also offers IP services for customers.

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## PREFACE

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### About this Document

This document is to describe the PCIe Gen5 Retimer IC and the corresponded control signals. In addition, it discusses how to apply the functions and illustrates the status register reported by these functions.

## 1. OVERVIEW

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### 1.1 General Description

The PS7202 is a 8-lane bidirectional high performance Retimer IC designed for Peripheral Component Interconnect Express (PCIe) 5.0 applications that supports up to 32 Gbps data rate. It is used to extend the reach and robustness of PCIe serial links over a variety of physical mediums, from motherboard, interconnect cables to more complex multi-connectors topologies.

The PS7202 integrates signal conditioning to compensate the channel attenuation and different TYPs of jitter, including random and deterministic jitter. The programmable setting can be applied using SMBus Interface. Additionally, the configuration data can be loaded through an external serial-EEPROM.

The PCIe Retimer supports diagnostic capabilities include receiver margining, eye open, error indicator and thermal monitor, in order to diagnose signal integrity issues for large scale enterprise and server deployment.

## 1.2 Features

- Compliant with PCIe 5.0 Base Spec
- Compliant with CXL 2.0
- Compliant with Intel publication PCI Express 5.0 Retimer Supplemental Features and Standard BGA Footprint
- Compliant with Intel publication PCI Express and Compute Express Link Low Latency Retimer Specification
- Link bifurcation supports 1x8, 2x4, 4x2, and other combinations enabling completely independent links
- Supports common clock, SRIS, and SRNS
- Supports power saving states: L1 (standby)
- Supports hot plug, lane margining and receiver eye generation
- Supports lane reversal and polarity inversion
- Supports JTAG debug and Reference Clock Out
- Integrated AC-coupling capacitors
- Supports SMBus configuration and external EEPROM configuration loading
- Extends reach to >40 dB at 32 GT/s
- Low-Latency Modes: <5 ns
- Supply voltage: 0.9V, 1.2 ~ 1.8V and 1.8V
- Junction temperature: -10°C ~ +110°C
- Package: FCCSP332(eCUF), 8.5 mm x 13.4 mm

## 1.3 Application

- Rack server
- Backplane reach extension
- Data Center and Storage
- Workstation

### 1.3.1 Server Motherboard Application

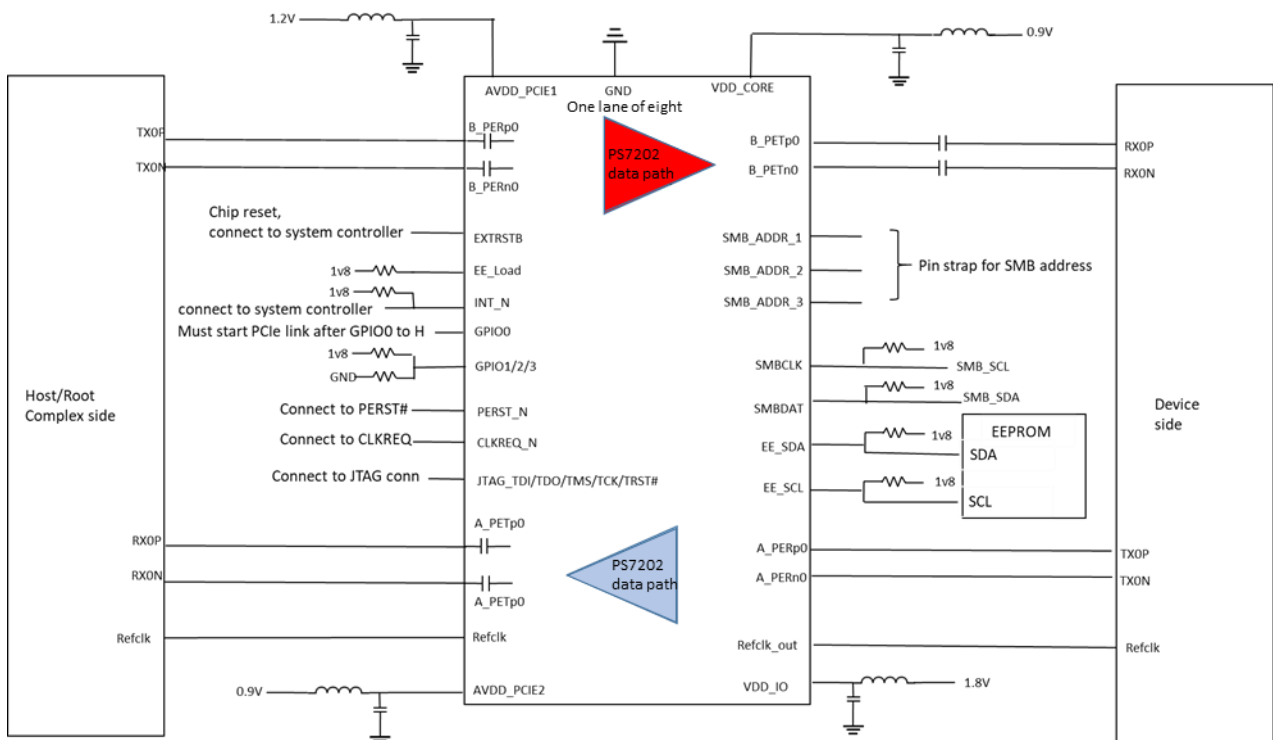


Figure 1: Simplified Schematic for PCIe 1-Lane Configuration

## 1.3.2 Backplane Application

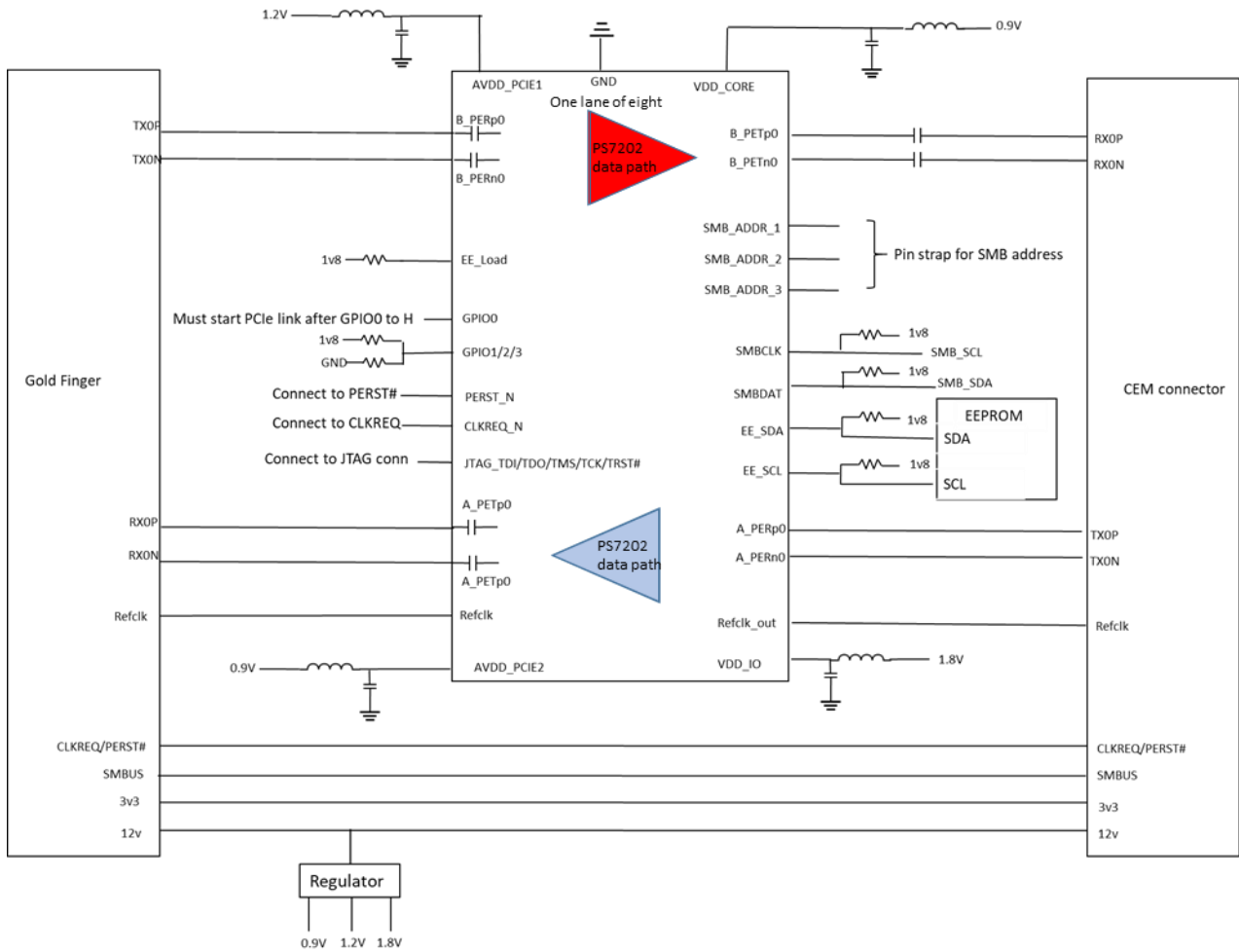


Figure 2: Simplified Schematic for PCIe 1-Lane Configuration

## 1.4 Retimer Latency

The PS7202 supports both normal latency mode and low latency mode. The normal latency mode meets PCIe Base Specification 5.0 and the low latency mode targets those system applications requiring low latency, etc. CXL. The retimer latency for Gen4 and Gen5 are listed in [Table 1](#).

Table 1: Retimer Latency

Symbol	Parameter	Test condition	MIN	TYP	MAX	UNIT
<b>V<sub>LAT-NORM</sub></b>	Normal Latency Mode	16.0 GT/s		124	128	Symbol times
				62	64	ns
		32.0 GT/s		144	256	Symbol times
				36	64	ns
<b>V<sub>LAT-LOW</sub></b>	Low Latency Mode	16.0 GT/s		<10		ns
		32.0 GT/s		<5		

## 1.5 Product Family Information

Table 2: Product Family

Part#	Equalization	PCIe	Lanes	Status
<b>PS7261</b>	>32 dB at 64 GT/s	Designed to support PCIe 6.0 up to 64Gbps	16 Lanes	Pre-Production
<b>PS7262</b>			8 Lanes	Pre-Production
<b>PS7201</b>	>40 dB at 64 GT/s	Designed to support PCIe 5.0 up to 32Gbps	16 Lanes	Production
<b>PS7202</b>			8 Lanes	Production

## 2. ORDERING INFORMATION

Table 3: Ordering Information

Part Number	Marking	Max. PCIe	Version	Package Type	Package Size	Packing
PS7202-74	PS7202-74	Gen5, CXL	AA	FC-CSP-332 (eCUF)	8.5mm x 13.4mm	Tray

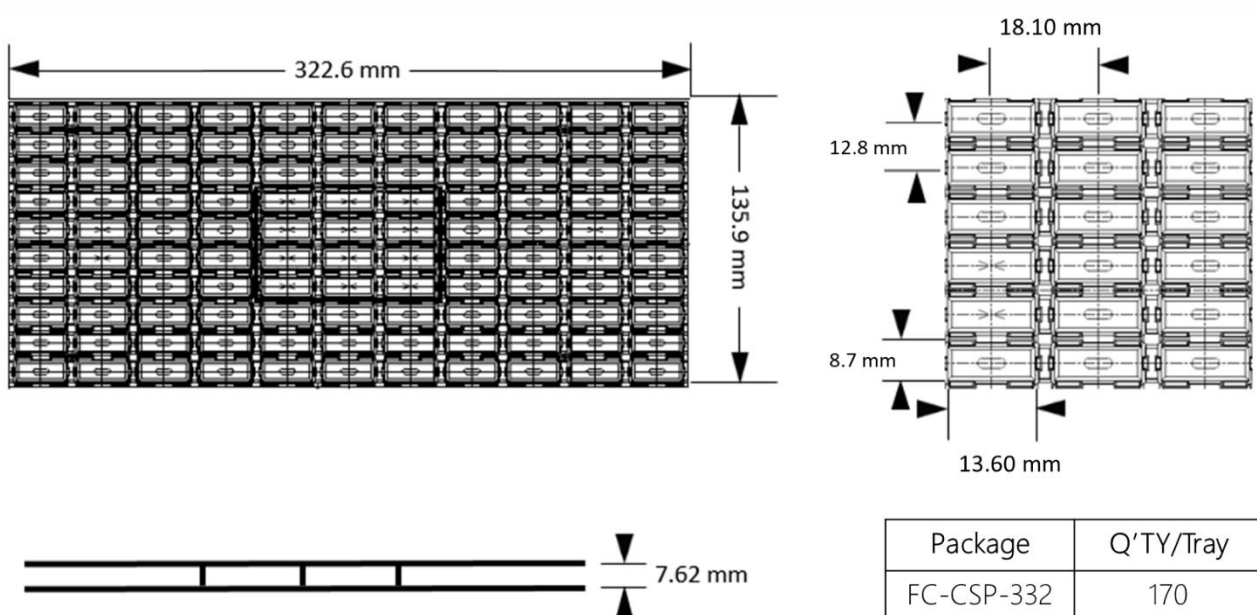
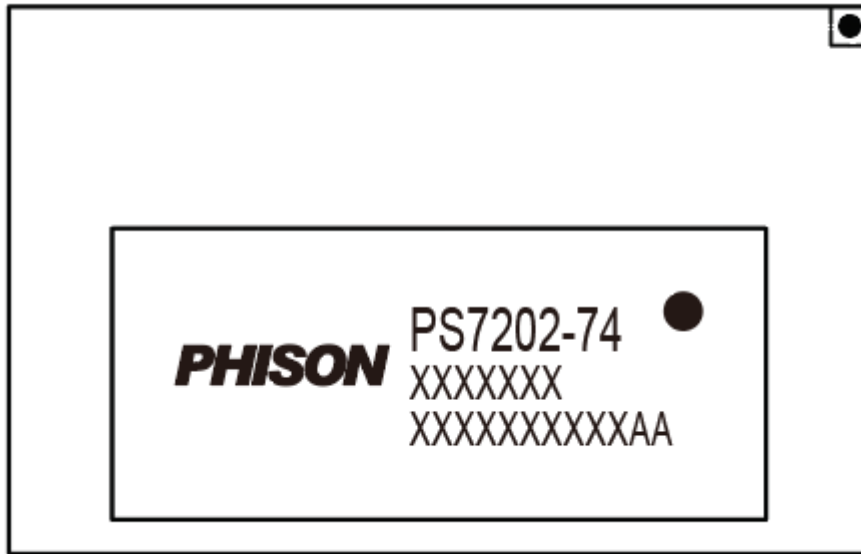


Figure 3: Tray Specification