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PHISON PS7261  
PCIE 6.0 RETIMER IC  
PRELIMINARY DATASHEET

V1.3 Mar. 3, 2026

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## REVISION HISTORY

Revision	Description	Draft Date
1.0	● Preliminary datasheet release	Feb. 26, 2026
1.3	● Minor Update	Mar. 3, 2026

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## PREFACE

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### About this Document

This document is to describe the PCIE Gen5 Retimer IC and the corresponded control signals. In addition, it discusses how to apply the functions and illustrates the status register reported by these functions.

### Definition of Acronyms and Abbreviations

Various acronyms and abbreviations are used in place of the full definition and the definitions of all acronyms and abbreviations are listed in Table 1 below:

Table 1: Definition of Acronyms and Abbreviations

Item	Definitions
PCIe	Peripheral Component Interconnect Express
EQ	Equalization
RX	Receiver
TX	Transmitter
FEXT	Far-End Cross Talk
NEXT	Near-End Cross Talk
RC	Root Complex
EP	Endpoint
FG	Flat Gain
AIC	Add-In Card
EVB	Evaluation Board
FW	Firmware
VUC	Vendor Unique Command

## 1. OVERVIEW

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### 1.1 General Description

The PS7261 is a 16-lane bidirectional high performance Retimer IC designed for Peripheral Component Interconnect Express (PCIe) 6.0 applications that supports up to 64 Gbps data rate. It is used to extend the reach and robustness of PCIe serial links over a variety of physical mediums, from motherboard, interconnect cables to more complex multi-connectors topologies.

The PS7261 integrates signal conditioning to compensate the channel attenuation and different TYPs of jitter, including random and deterministic jitter. The programmable setting can be applied using SMBus Interface. Additionally, the configuration data can be loaded through an external serial-EEPROM/SPI flash.

The PCIe Retimer supports diagnostic capabilities include receiver margining, eye open, error indicator and thermal monitor, in order to diagnose signal integrity issues for large scale enterprise and server deployment.

### 1.2 Features

- Compliant with PCIe 6.0 Base Spec
- Compliant with CXL 3.0
- Compliant with Intel publication PCI Express 6.0 Retimer Supplemental Features and Standard BGA Footprint
- Link bifurcation supports 1x16、2x8、4x4、8x2, and other combinations enabling completely independent links
- Supports common clock, SRIS, and SRNS
- Supports power saving states: L1 (standby)
- Supports hot plug, lane margining and receiver eye generation
- Supports lane reversal and polarity inversion
- Supports JTAG debug and Reference Clock Out
- Supports low latency mode
- Integrated AC-coupling capacitors
- Supports SMBus configuration and external EEPROM/SPI flash configuration loading
- Extends reach to >36 dB at 64 GT/s
- PRBS Generator and checker
- IEEE 1149.1 & IEEE 1149.6 AC-JTAG boundary scan
- Junction temperature: -10°C ~ +110°C
- Package: FCCSP354(eCUF), 8.9 mm x 22.8 mm

## 1.3 Application

- GPU/AI system
- PCIe riser card and backplane trace extension
- NVMe storage server
- Rack server
- Workstation

## 2. APPLICATION AND IMPLEMENTATION

### 2.1 Typical Applications

#### 2.1.1 Server Motherboard Application

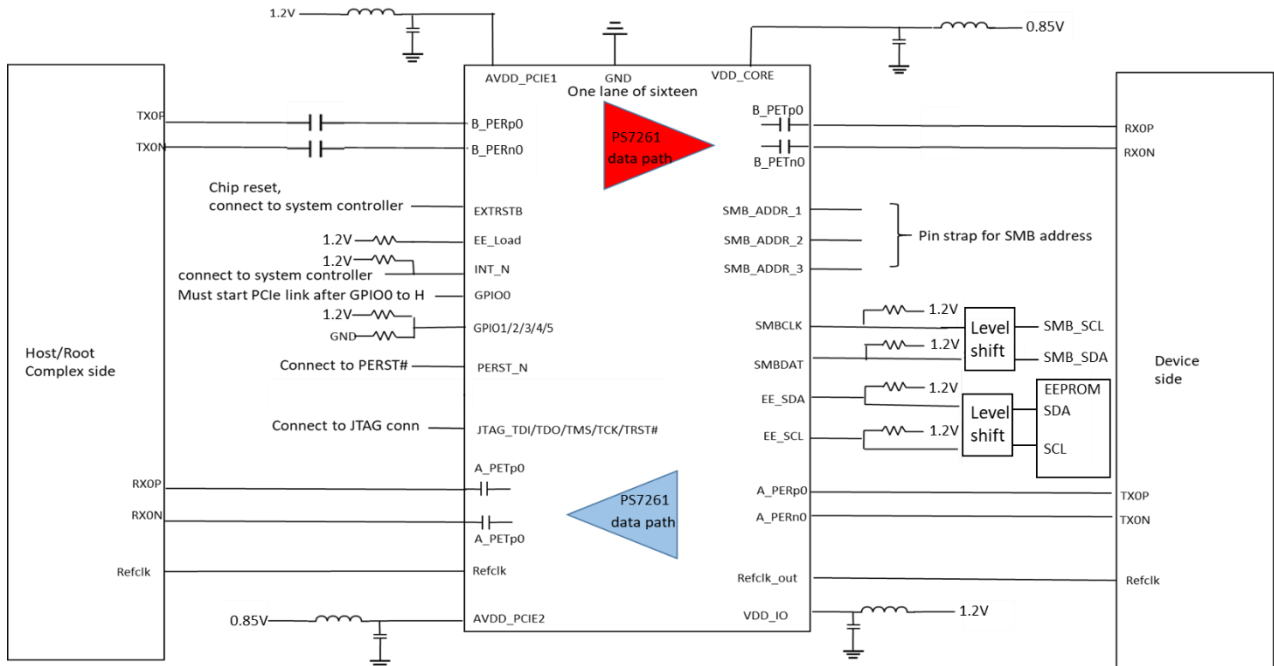


Figure 1: Simplified Schematic for PCIe 1-Lane Configuration

## 2.1.2 Backplane Application

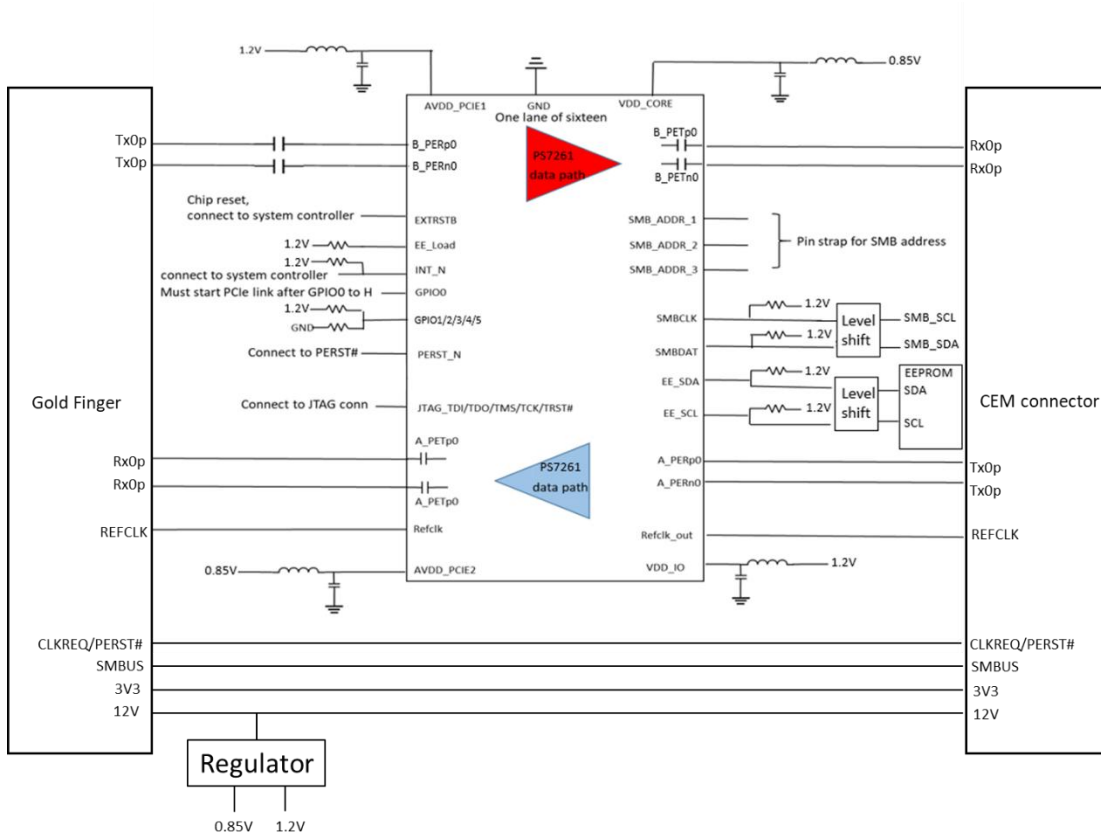


Figure 2: Simplified Schematic for PCIe 1-Lane Configuration

## 3. ORDERING INFORMATION

Table 2: Ordering Information

Part Number	Marking	Max. PCIe	Version	Package Type	Package Size	Packing
PS7261-77	PS7261-77	Gen6, CXL	AA	FC-CSP-354 (eCUF)	8.9mm x 22.8mm	Tray

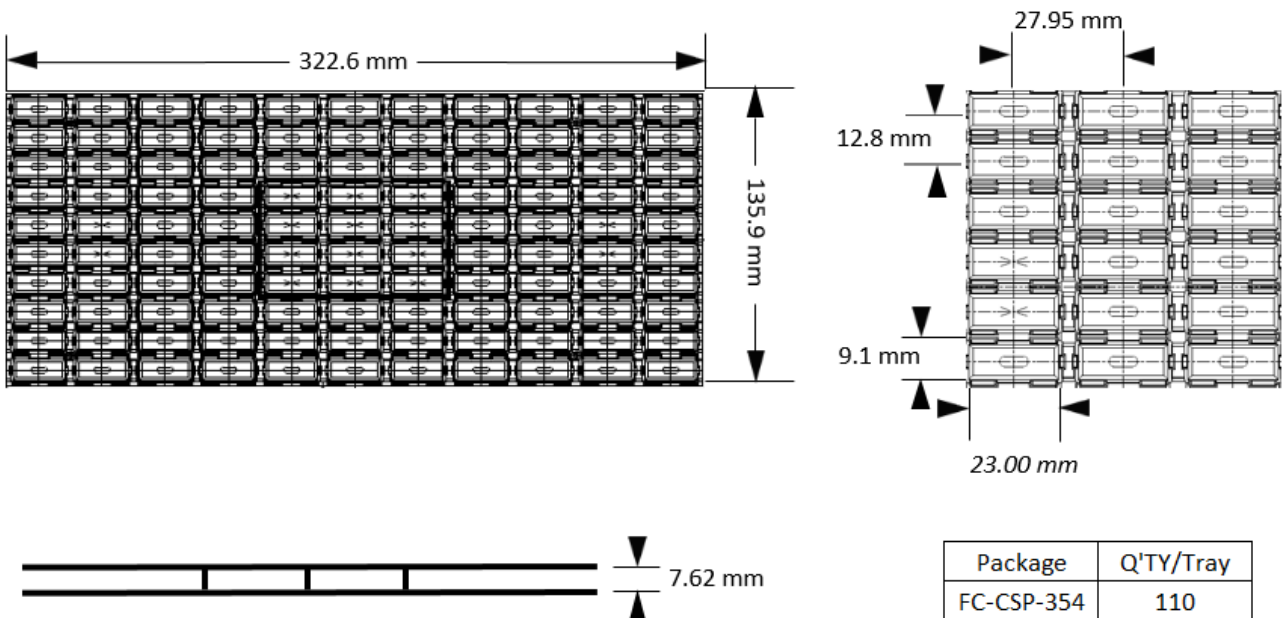
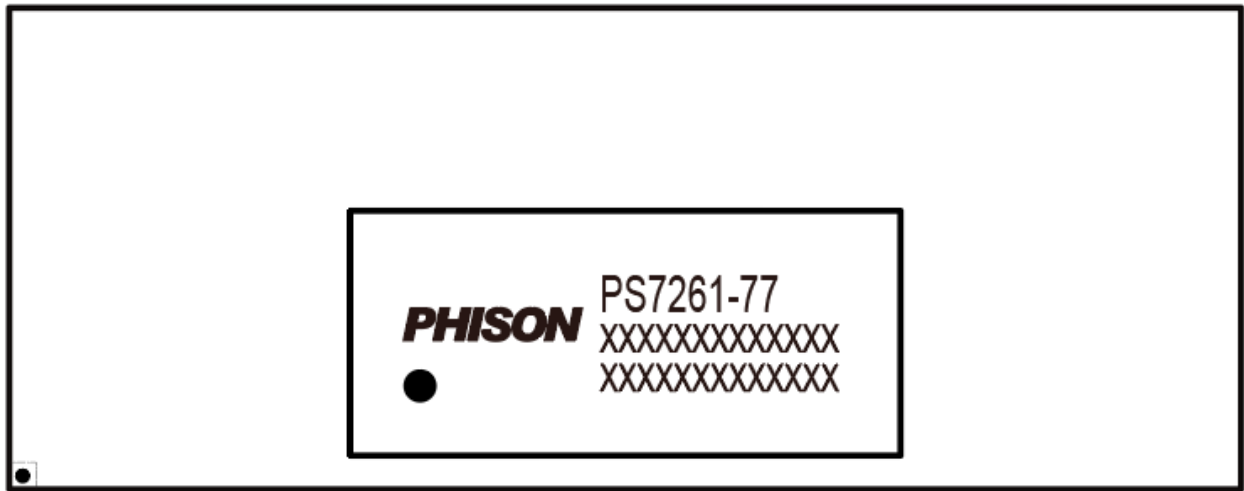


Figure 1: Tray Specification